Si5346-EVB

Si5346 Evaluation Board User's Guide

Description

The Si5346-EVB is used for evaluating the Si5346 Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier. The Si5346 contains 2 independent DSPLLs in a single IC with programmable jitter attenuation bandwidth on a per DSPLL basis. The Si5346-EVB supports 4 independent input clocks and 4 independent clock outputs via on-board SMA connectors. The Si5346-EVB can be controlled and configured using the ClockBuilderPro™ (CBPro™) software tool. Test points are provided on-board for external monitoring of supply voltages.

EVB Features

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL allows standalone or holdover mode of operation on the Si5346.
- CBPro™ GUI programmable V_{DD} supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro™ GUI programmable V_{DDO} supplies allow each of the 4 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro™ GUI allows control and measurement of voltage, current, and power of V_{DD} and all 4 V_{DDO} supplies.
- Status LEDs for power supplies and control/status signals of Si5346.
- SMA connectors for input clocks, output clocks, and optional external timing reference clock.

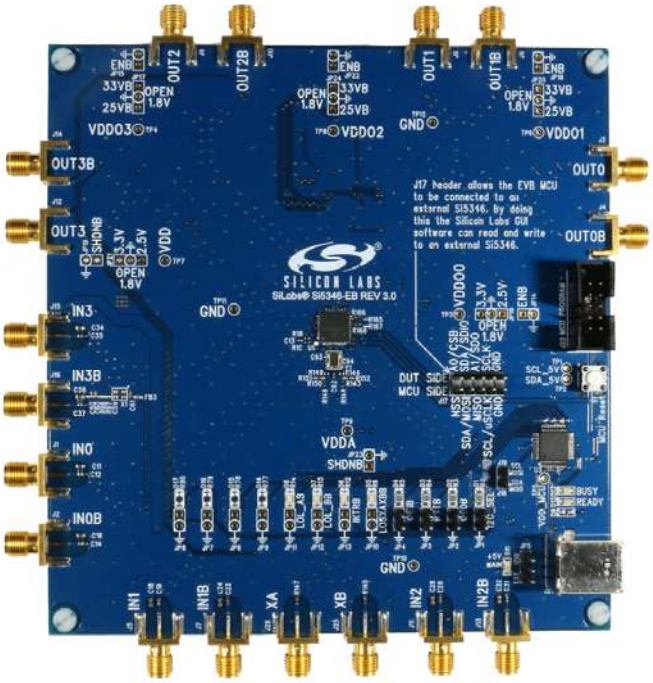


Figure 1. Si5346 Evaluation Board

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1. Si5346-EVB Functional Block Diagram

Below is a functional block diagram of the Si5346-EVB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See section “3. Quick Start” or section “9. Installing ClockBuilderPro (CBPro) Desktop Software” for more information.

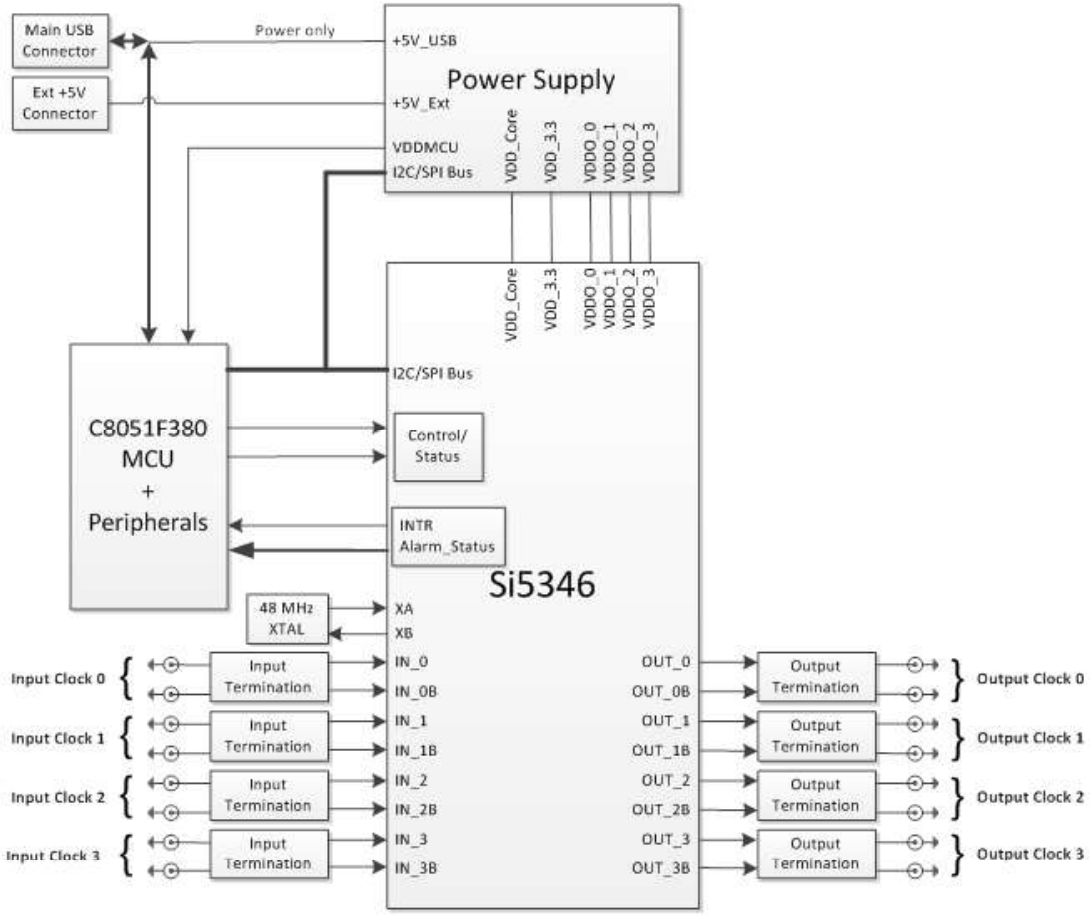


Figure 2. Si5346-EVB Functional Block Diagram

2. Si5346-EVB Support Documentation and ClockBuilderPro Software

All Si5346 schematics, BOMs, User's Guides, and software can be found online at the following link:
http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

3. Quick Start

1. Install ClockBuilderPro™ desktop software from http://www.silabs.com/CBPro.
2. Connect a USB cable from Si5346-EVB to the PC where the software was installed.
3. Leave the jumpers as installed from the factory, and launch the ClockBuilderPro software.
4. You can use ClockBuilderPro™ to create, download, and run a frequency plan on the Si5346-EVB.
5. For the Si5346 data sheet, go to http://www.silabs.com/timing.

4. Jumper Defaults

Si5346 EVB Jumper Defaults					
Location	Type	I = Installed 0 = Open	Location	Type	I = Installed 0 = Open
JP1	2 pin	I			
JP2	2 pin	I			
JP3	2 pin	O			
JP4	2 pin	I			
JP5	**3 pin**	1 to 2 (USB)			
			J17	**5x2 Hdr**	All 5 installed

Refer to the Si5346 EVB schematics for the functionality associated with each jumper.

5. Status LEDs

Si5346 EVB Status LEDs			
Location	**Silkscreen**	**Color**	**Status Function Indication**
D5	LOS_XAXBB	Blue	XA/XB Loss of Signal indicator
D6	INTRB	Blue	MCU INTR (Interrupt) active
D7	LOL_BB	Blue	DSPLL A Loss of Lock indicator
D8	LOL_AB	Blue	DSPLL B Loss of Lock indicator
D11	+5V MAIN	Green	Main USB +5V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

D5, D6, D7, and D8 are status LEDs indicating the device alarms currently asserted. D11 is illuminated when USB +5 V supply voltage is present. D12 and D13 are status LEDs showing on-board MCU activity.

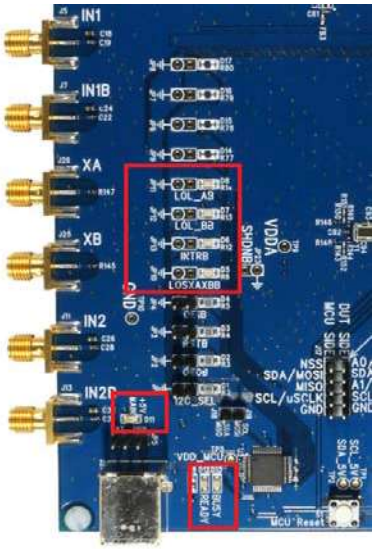


Figure 3. Status LEDs

6. Clock Input Circuits (INx/INxB)

The Si5346-EVB has eight SMA connectors (IN0/IN0B–IN3/IN3B) for receiving external clock signals. All input clocks are terminated as shown in Figure 4 below. Note input clocks are AC coupled and 50 ohm terminated. This represents 4 differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5346 data sheet. Typically a 0.1 µF DC block is sufficient, however, 10 µF may be needed for lower input frequencies. Note that the EVB is populated with both DC block capacitor values.

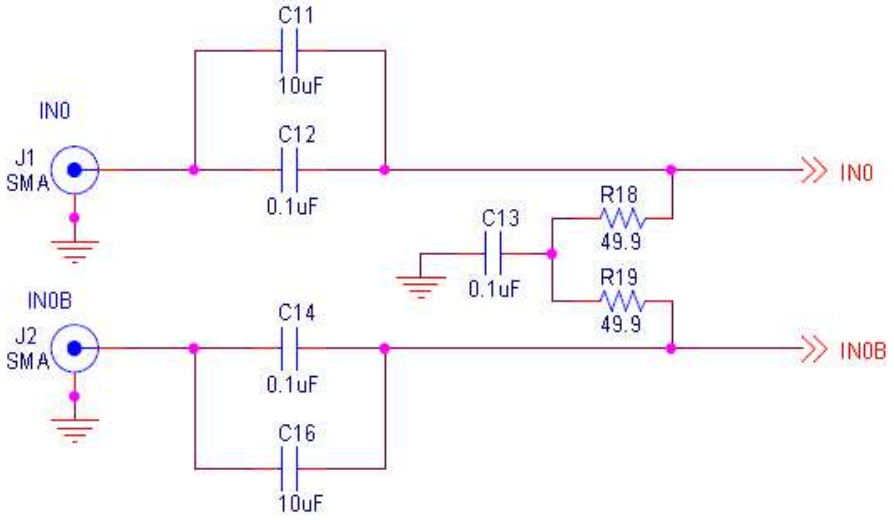


Figure 4. Input Clock Termination Circuit

7. Clock Output Circuits (OUTx/OUTxB)

Each of the eight output drivers (4 differential pairs) is AC coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 5 below. The output signal will have no DC bias. If DC coupling is required, the AC coupling capacitors can be replaced with a resistor of appropriate value. The Si5346-EVB provides an L-network at OUT0/OUT0B output pins for optional output termination resistors. Note that components with schematic "**NI**" designation are not normally populated.

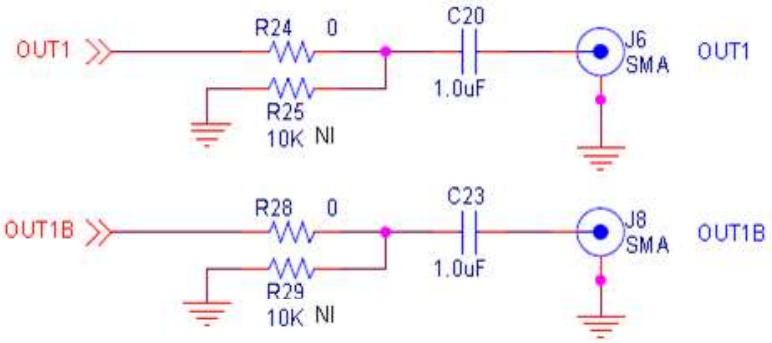


Figure 5. Output Clock Termination Circuit

8. External Reference Clock Input Circuit (XA/XB)

The Si5346 EVB supports either XTAL or external reference clock on XA/XB. By default, the XTAL is populated. If a reference clock is required for testing, remove Y1 and place C93/C94. A low-jitter reference clock can then be applied to J25/J26. Note that XA/XB is the jitter reference for the device. Jitter performance at the output of the Si5346 will depend on the jitter performance of the reference clock at XA/XB.

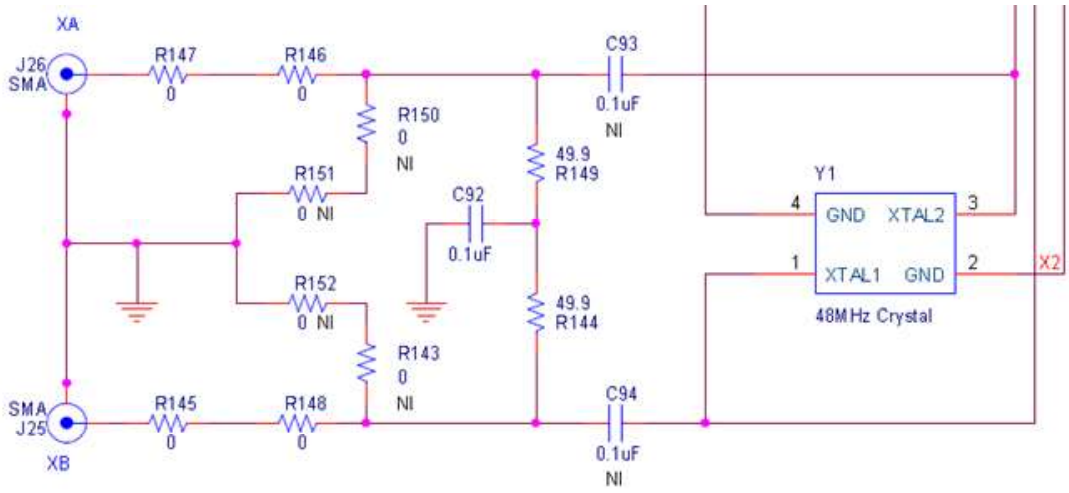


Figure 6. External Reference Clock Termination Circuit

9. Installing ClockBuilderPro (CBPro) Desktop Software

To install the CBOPro software on any **Windows 7** (or above) PC:

Go to http://www.silabs.com/CBPro and download ClockBuilderPro software.

Installation instructions and User's Guide for ClockBuilderPro™ can be found at the download link shown above. Please follow the instructions as indicated.

10. Using the Si5346 EVB

10.1. Connecting the EVB to Your Host PC

Once ClockBuilderPro™ software is installed, connect to the EVB with a USB cable as shown below.

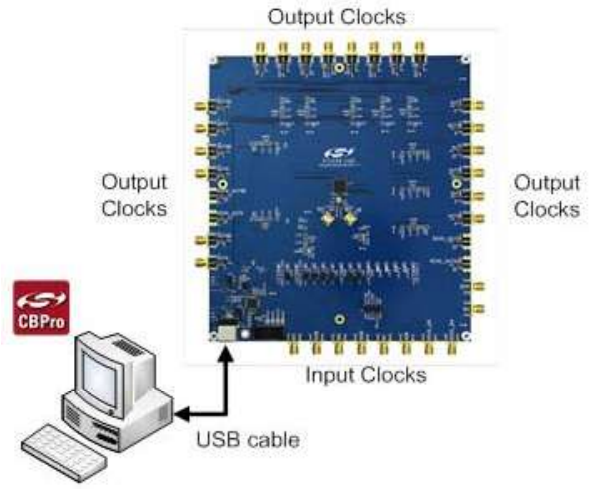


Figure 7. EVB Connection Diagram

10.2. Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is ***not*** needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5346-EVB schematic for details.

10.3. Overview of ClockBuilderPro™ Applications

The ClockBuilderPro™ installer will install **two** main applications:



Figure 8. Application #1: ClockbuilderPro Wizard

Use the CBPro Wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming



Figure 9. Application #2: EVB GUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5346)
- Control the EVB's regulators
- Monitor voltage, current, power on the EVB

10.4. Common ClockBuilderPro™ Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5346 EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

10.5. Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch **ClockBuilder Pro** by clicking on this icon on your PC's desktop.



Figure 10. ClockBuilderPro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.



Figure 11. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.



Figure 12. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5346 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.



Figure 13. Writing Design Status

After CBPro writes the default plan to the EVB, click on “Open EVB GUI” as shown below.

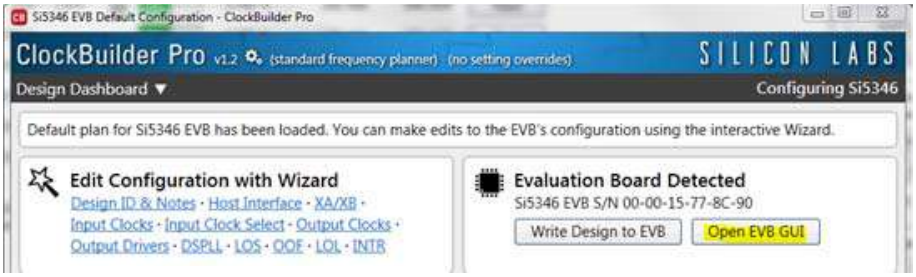


Figure 14. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device’s default CBPro project file created by Silicon Labs, as shown below.

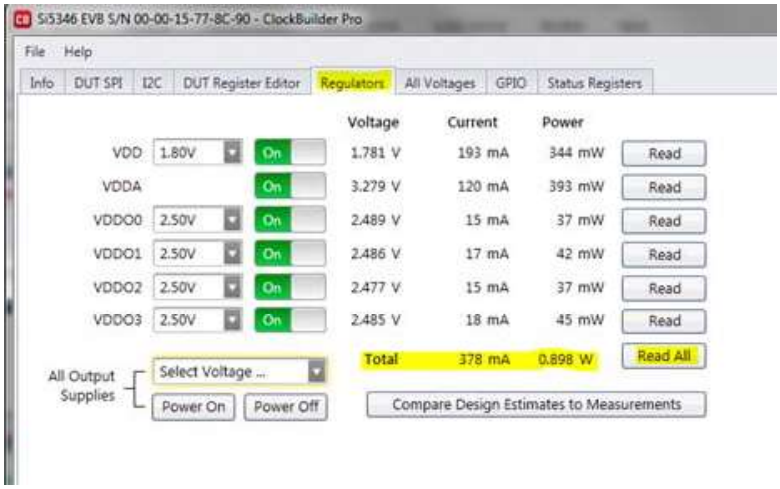


Figure 15. EVB GUI Window

10.5.1. Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled “INx/INxB”) located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting “Off” then “On” of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT’s register space, you must go back to the Wizard’s main menu and select “Write Design to EVB”:

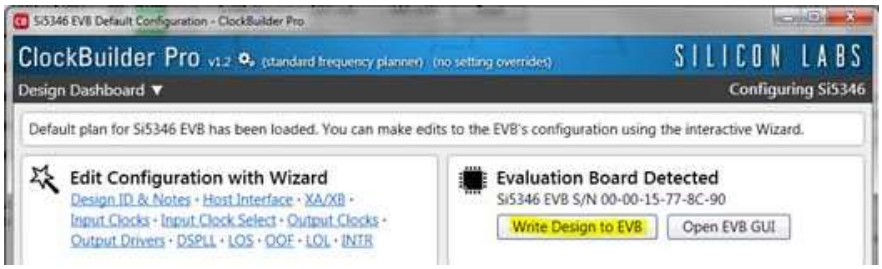


Figure 16. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.



Figure 17. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

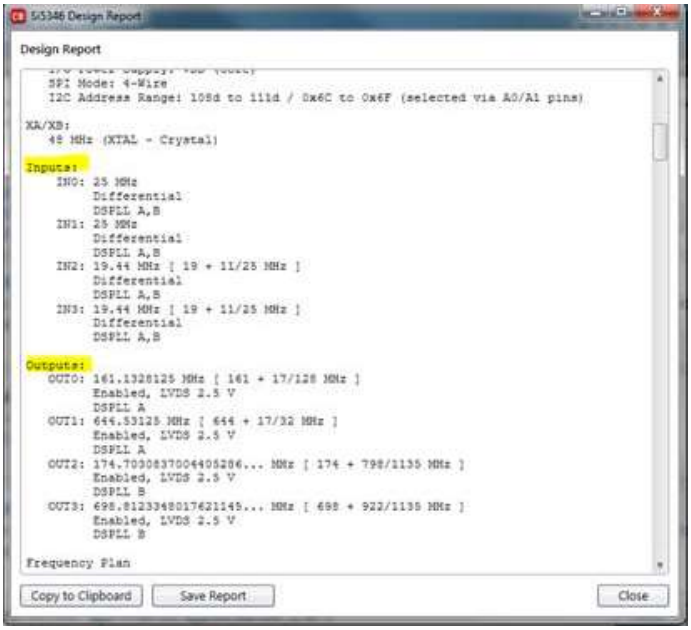


Figure 18. Design Report Window

10.5.2. Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in “locked” mode.

10.6. Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the “default” configuration using the CBPro Wizard, click on Edit Configuration with Wizard:



Figure 19. Edit Configuration with Wizard

You will now be taken to the Wizard’s step-by-step menus to allow you to change any of the default plan’s operating configurations.



Figure 20. Design Wizard

Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.



Figure 21. Writing Design Status

10.7. Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.



Figure 22. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file).design file in the Windows file browser.

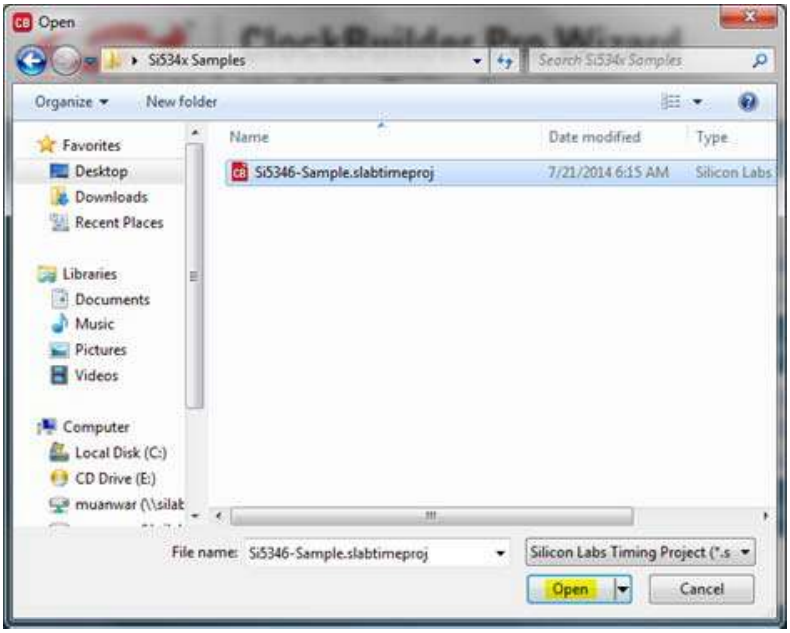


Figure 23. Browse to Project File

Select Yes when the WRITE DESIGN to EVB popup appears:



Figure 24. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.8. Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:

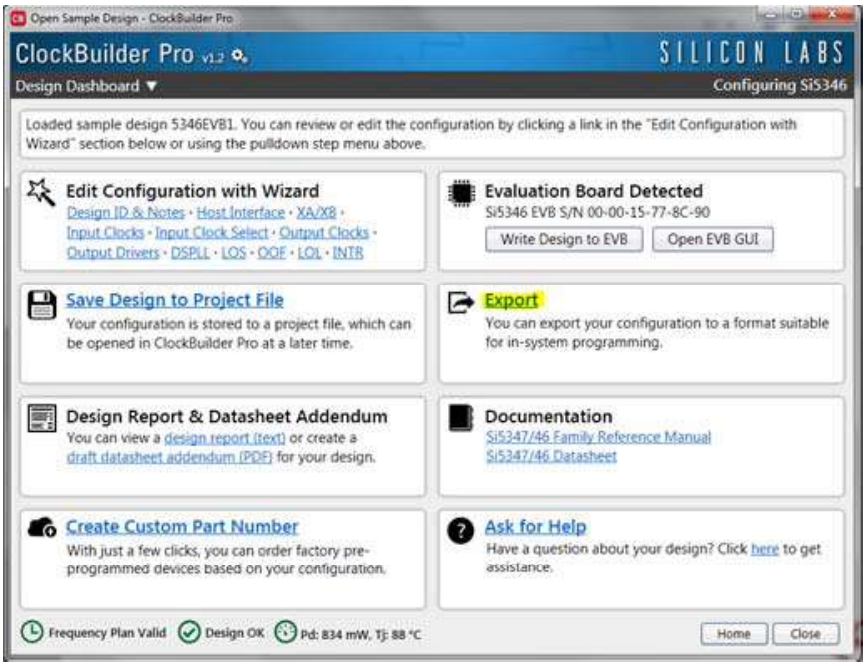


Figure 25. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

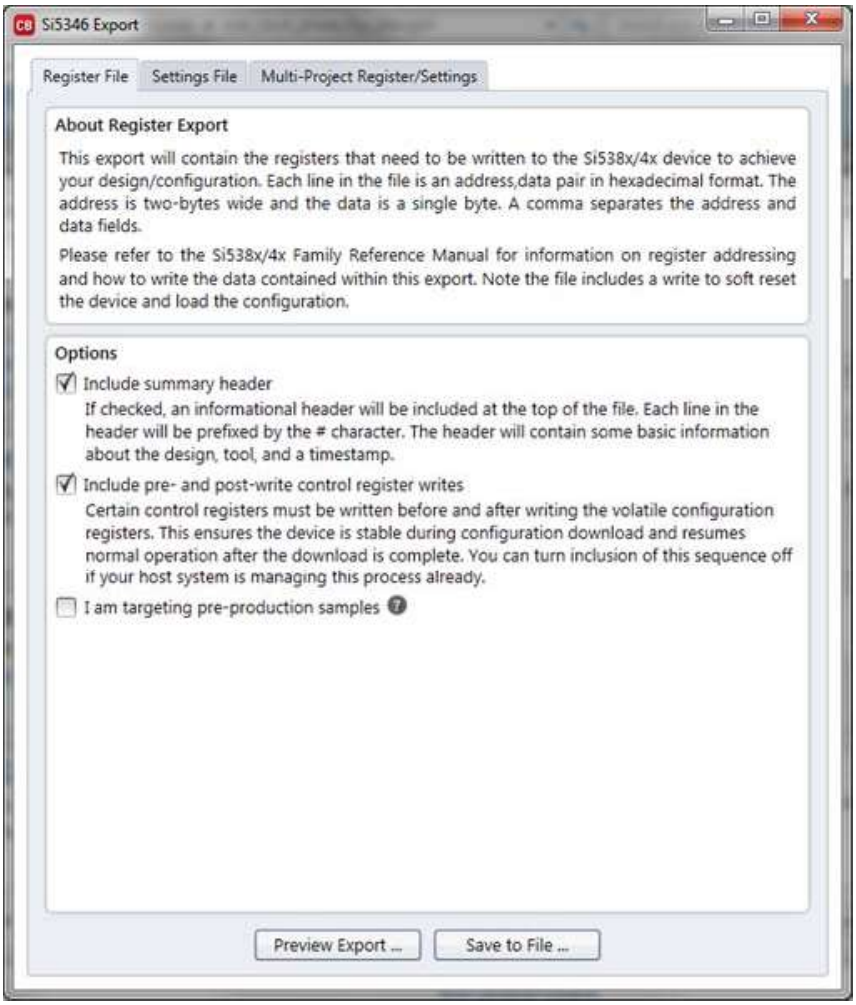


Figure 26. Export Settings

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5346 using ClockBuilderPro on the Si5346 EVB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5346 RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

12. Si5346-EVB Schematic and Bill of Materials (BOM)

The Si5346 EVB Schematic and Bill of Materials (BOM) can be found online at

http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

Note: Please be aware that the Si5346-EVB schematic is in **OrCad Capture** *hierarchical format* and not in a typical "flat" schematic format.



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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